Short duration undervoltage response test

1. General test and reporting requirements

1.1 General

The intention of this test procedure is to verify the behaviour of an inverter energy system during a short-duration undervoltage disturbance. The inverter should sufficiently demonstrate the ability to remain in continuous operation through a 220 ms duration voltage dip to 50 V. This test should be applied in conjunction with existing product certification testing for compliance with AS/NZS 4777.2:2015 and has been developed as a supplementary test. All definitions throughout are according to AS/NZS 4777.2.

Where possible the undervoltage (V<) trip level from the original AS/NZS 4777.2:2015 certification should be noted. If this value is not available, then the undervoltage (V<) test as described in AS/NZS 4777.2:2015 Appendix G2.2 should be performed to determine the value.

This test is used to verify:

- The undervoltage trip delay and maximum disconnection time for a short-duration undervoltage event, and
- The withstand capability for a short-duration undervoltage event that occurs within the trip delay time.

This test shall be repeated three times to confirm requirements in Section 2.4 are met.

1.2 Test conditions

Unless otherwise specified by the test procedure, the testing conditions for each test shall be such that:

a) the average r.m.s. current on each phase is within ±5 % of the intended test point; and

b) the average r.m.s. voltage on each phase is within ±1 % of the grid test voltage.

In the case of a three-phase supply, the angle between the fundamental voltages of each pair of phases shall be maintained at 120 ± 1.5°. The average r.m.s. voltages between each pair of phases shall be maintained within ±1 %.

The grid test voltage shall be 230 V a.c. phase to neutral, 50 ± 0.1 Hz.

1.3 Inverter setup

Each inverter that is to be tested shall have its device settings and configurations set to the default set-points required by AS/NZS 4777.2:2015, as they would be for operation in an installation. Once the default settings are selected, the power quality response mode settings should be set according to the Energy Networks Australia[1] recommended default power quality response modes Tables 4a, 4b and 4c.

If the inverter is required to be used with an external device or devices, such as external automatic disconnection devices or dedicated isolation transformers, the inverter shall be configured in combination with these devices for all tests. The combinations tested shall be documented in the test report.

Before commencement of the test, all model information and specific information concerning the version of software, firmware and hardware used by the inverter shall be recorded. This information shall be provided in the test report. High speed monitoring data records shall be kept and archived; photographs taken to be included in the test report such that the model tested can be verified. The test data and information shall be made available upon request.

[1] ENA Power Quality Response Mode Settings. https://www.energynetworks.com.au/miscellaneous/power-quality-response-mode-settings/.

1.4 Grid source

Either a real grid or a simulated test grid shall be used in the testing.

Whether a real grid or simulated test grid is used, the impedance of the test point shall be rated appropriate to the rating of the inverter or combination of inverters under test. The impedance of the test point should not cause a voltage rise greater than 0.5 % of the grid test voltage at the rated current output of the device under test.

NOTE: This is to ensure that the application of the inverter in a customer installation will not adversely affect the quality of supply to the customer.

The type and impedance of the source shall be declared in the test report for each test performed.

During the tests, the steady-state voltage of the real or simulated test grid shall not vary by more than ±1 % of the grid test voltage. The grid test voltage shall be set as required by each test.

For tests requiring step changes in voltage, the simulated test grid shall be capable of being stepped at least 0.5 times the smallest step required for testing, to determine the set-points with required accuracy.

The real grid or a simulated test grid should be free from harmonic distortion which could interfere with testing. The voltage harmonic distortions of the real or simulated test grid shall be less than the limits specified in the table below.

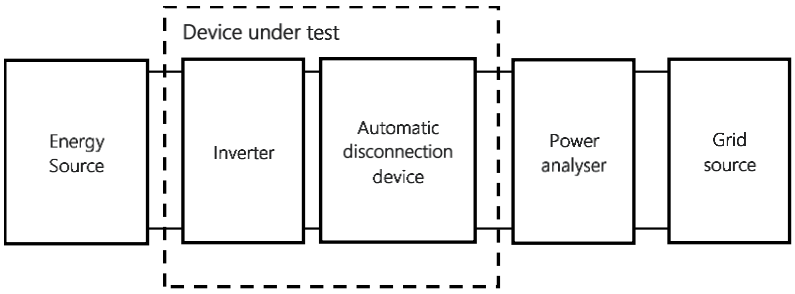
Harmonic order number	Limit based on percentage of fundamental
3	0.9 %
5	0.4 %
7	0.3 %
9	0.2 %
Even harmonics 2–10	0.2 %
11–50	0.1 %
Total harmonic distortion (to the 50th harmonic)	5 %

2. Test procedure

2.1 General

The following test procedure steps should be completed sequentially. For each of these tests the inverter and automatic disconnection device shall be connected into a test circuit equivalent to that shown in Figure 1.

Figure 1 Test circuit for voltage limits



NOTE: The above test circuit applies to a single-phase system. To test a three-phase system, an equivalent three-phase circuit is required.

2.2 Undervoltage (V<) disconnection test in response to event duration exceeding trip delay time

The disconnection time for the protective function undervoltage (180 V) for a voltage step shall be confirmed. The procedure shall be as follows:

(a) Set the grid source equal to the grid test voltage. Vary the energy source until the a.c. output of the device under test equals 50 ± 5 % of its rated current output.

NOTE: For three-phase inverters or inverter combinations, the required inverter output is based on the per phase inverter current rating.

(b) Step the grid source voltage down to 177.5 V (2.5 V below 180 V) with the step change completed within 2 ms and occurring at the zero crossing of the grid source voltage. Record the time interval between the start of the voltage step and the device under test disconnecting from the grid source.

NOTE: For three phase systems, the test shall be conducted at the zero-crossing for each phase individually, and additionally for all three phases stepped together at the zero-crossing for one of the phases.

(c) Adjust the grid source to return the voltage to the grid test voltage. Record the reconnection time (the time taken for the device under test to reconnect to the grid source).

2.3 Undervoltage (V<) withstand test in response to event duration of less than trip delay time

The trip delay requirement for the protective function undervoltage 1 (V <) of 180 V for a voltage step shall be confirmed. The procedure shall be as follows:

(d) Set the grid source equal to the grid test voltage. Vary the energy source until the a.c. output of the device under test equals 50 ± 5 % of its rated current output.

NOTE: For three-phase inverters or inverter combinations, the required inverter output is based on the per phase inverter current rating.

(e) Record the stabilised active power output.

(f) Step the grid source voltage down to 50 V with the step change completed within 2 ms and occurring at the zero crossing of the grid source voltage, remain at 50 V for 220 ms. Increase the grid source voltage to the grid test voltage with the step change completed within 2 ms and occurring at the zero crossing of the grid source voltage. Record the time interval between each voltage step passing through 180 V (i.e. the duration for which voltage lies below 180 V).

NOTE: For three phase systems, the test shall be conducted at the zero-crossing for each phase individually, and additionally for all three phases stepped together at the zero-crossing for one of the phases.

(g) After 1 second, record the active power output, and confirm it is equal to that recorded at Step (e) ± 4 %.

NOTE: There is no defined behaviour of the inverter during the simulated fault. Monitor and recording at this stage is to better understand the anticipated inverter response.

2.4 Criteria for acceptance

(1) The disconnection time recorded at Step (c) shall be greater than the trip delay time of AS4777.2:2015 of 1 s and less than the disconnection time of AS4777.2:2015 of 2 s.

(2) The device under test shall remain connected for the duration of Step (f).

(3) At Step (g) the device under test shall have recovered its active power output to that recorded at Step (e) ± 4 % within 1 second.

2.5 Test report specifications

For each test performed, the results specified in the test procedure and criteria for acceptance shall be recorded and displayed in the test report. The report shall include time-series plots that shows the instantaneous and RMS voltage waveform and the power output of the device under test over the duration of each test (A1.5.2 and A1.5.3). The presented waveforms shall demonstrate that the inverter appropriately disconnected after 1 second, and that the inverter remained connected and recovered to a stable output for a disturbance of less than 1 second. The test report should clearly indicate whether the inverter met or failed each acceptance criteria.

3. Accreditation

The testing facility must have the technical competence to undertake the test and be accredited by either:

- The Australian National Association of Testing Authorities (NATA), or
- The International Accreditation New Zealand (IANZ); or
- By accreditation bodies that are signatories to the International Laboratory Accreditation Cooperation Mutual Recognition Arrangements (ILAC MRA).

4. Conformance

Once the testing is complete, the test report is to be provided to the CEC for conformance approval and listed on to CEC Approved Inverter Listing[2].

For any further enquiries, please contact AEMO's DER Program via

- DERProgram@aemo.com.au or
- call 1300 236 600.

[2] https://www.cleanenergycouncil.org.au/industry/products/inverters/approved-inverters